Remarks

The final Office Action dated May 18, 2009, notes the following: a rejection of claims 1, 5 and 7 under 35 U.S.C. § 102(b) over Thuringer (U.S. Patent No. 6,498,404); a rejection of claims 2-4 under 35 U.S.C. § 103(a) over the '404 reference in view of the Patterson reference ("Computer Architecture: A Quantitative Approach"); and a rejection of claim 6 under 35 U.S.C. § 103(a) over the '404 reference. Claims 8-14 are noted as being substantially similar to claims 1-7 and are rejected. In this discussion set forth below, Applicant does not acquiesce to any rejection or averment in this Office Action unless Applicant expressly indicates otherwise.

Applicant respectfully traverses the § 102(b) and § 103(a) rejections because the cited Thuringer '404 reference either alone or in combination with the Patterson reference lacks correspondence. For example, neither of the asserted references teaches the claimed invention "as a whole" (§ 103(a)) including aspects regarding, *e.g.,* pairs of processing signals coming into and out of respective ones of the processing circuits. In contrast, at page 4, the Office Action acknowledges that the '404 reference has only two signals input to an AND gate. As a further example, neither reference teaches aspects regarding activity information derived from each pair of processing signals. In contrast, the '404 reference teaches an AND gate that outputs a signal from which no activity information can be derived as claimed. Because neither reference teaches these aspects, no reasonable interpretation of the asserted prior art, taken alone or in combination, can provide correspondence. As such, the rejections fail.

Applicant further traverses the § 103 rejection of claims 2-4 because the cited references teach away from the Office Action's proposed combination. Consistent with the recent Supreme Court decision, M.P.E.P. § 2143.01 explains the long-standing principle that a § 103 rejection cannot be maintained when the asserted modification undermines either the operation or the purpose of the main ('404) reference - the rationale being that the prior art teaches away from such a modification. *See KSR Int'l Co. v. Teleflex, Inc.*, 127 S. Ct. 1727, 1742 (2007) ("[W]hen the prior art teaches away from combining certain known elements, discovery of a successful means of combining them is more likely to be non-obvious."). Applicant submits that the combination would render the invention inoperable because the '404 reference is an asynchronous circuit,

whereas the Patterson teaching (relied upon) in the Office Action is a synchronous approach; the two approaches are inoperable as asserted. Under M.P.E.P. § 2143.01, the rejections cannot be maintained.

Applicant incorporates by reference each of the arguments presented in the previously filed Office Action Response, as these arguments continue to be applicable. For example, the '404 reference teaches that AND gate 8 (*i.e.,* the asserted activity monitoring circuit) only receives the complements of the signals input to AND gate 5 (*i.e.,* the asserted processing circuit), instead of receiving multiple pairs of processing signals from different respective processing circuits as in the claimed invention. *See, e.g.,* Figure 2, Col. 1:45-65, and Col. 2:39-54. The AND gate 8 also does not receive any processing signals coming out of AND gate 5. Moreover, since AND gate 8 only receives signals from a single processing circuit (*i.e.,* AND gate 5), AND gate 8 does not derive a combined activity signal indicative of a sum of power supply currents that are consumed by multiple processing circuits as does Applicant's activity monitoring circuit.

In addition, Applicant submits that the Office Action appears to be improperly maintaining that AND gate 8 also corresponds to Applicant's current drawing circuit. Since AND gate 8 only receives signals from a single processing circuit, AND gate 8 does not draw a current responsive to the sum of power supply currents that are consumed by multiple processing circuits as does Applicant's current drawing circuit. Furthermore, Applicant maintains that the Office Action's apparent assertion that AND gate 8 corresponds to both the activity monitoring circuit and the current drawing circuit of the claimed invention is illogical because a single element cannot correspond to Applicant's two separate elements, one of which is controlled responsive to a signal produced by the other.

These arguments have not been properly addressed as required in M.P.E.P. § 707.07(f).

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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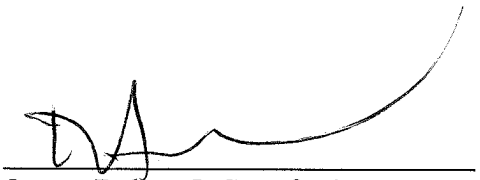
By: 

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